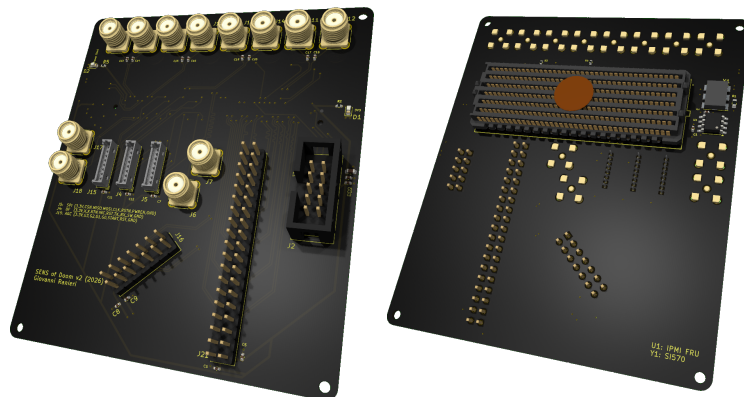


# SENS of Doom

## 1 Overview

- FMC+ Passive Adapter for ZCU208
- GTY High-Speed Differential Transceivers
- 2kB I2C EEPROM
- 10-810 MHz I2C Low-Jitter XO Clock Generator
- JTAG Debug
- Fully Interfaced for Siverts EVK06005



## 2 Description

### 2.1 Introduction

SENS of Doom is a passive breakout adapter that mates with the FMC+ HPC connector of the AMD/Xilinx ZCU208 evaluation board, and exposes the FPGA-side I/O to the user through a set of accessible interfaces (pin headers, SMA connectors, JTAG, I<sup>2</sup>C). The intended end-application is to interface the Siverts EVK06005 Phased Array module to the ZCU208 through the FMC+, so most of the design effort is concentrated on preserving signal integrity for high-speed pairs and on routing the control/clocks/RF interfaces required by such a module.

The ZCU208 is a powerful evaluation board. It features a Zynq UltraScale+ MPSoC XCZU48DR. The ZCU208 exposes a FMC+ connector developed by ANSI/VITA (VMEbus International Trade Association), and follows the standard 57.4. The FMC+ is an upgrade on the FMC (standard 57.1) connector, which includes more pins and capabilities. The FMC+ distinguishes the Carrier (C), which is the Master board, and the Mezzanine (M), the daughter board (here the PCB). Pins carrying data that are not bidirectional have the suffix M2C (Mezzanine to Carrier) or C2M (Carrier to Mezzanine) to differentiate the direction of signals. Because most of the pins are made differential, a suffix P/N is included (for Positive and Negative ends). Differential signaling is a method for electrically transmitting information using two complementary signals. The receiver measures the voltage difference between them, not the absolute voltage, allowing for better noise immunity and higher speeds.

SENS of Doom is designed specifically to interface with Siverts EVK06005 Phased Arrays via its 8-pins Molex row connectors.

### 2.2 Block Diagram

SENS of Doom is structured around the FMC+ connector. Figure [1] shows the high-level structure of SENS of Doom

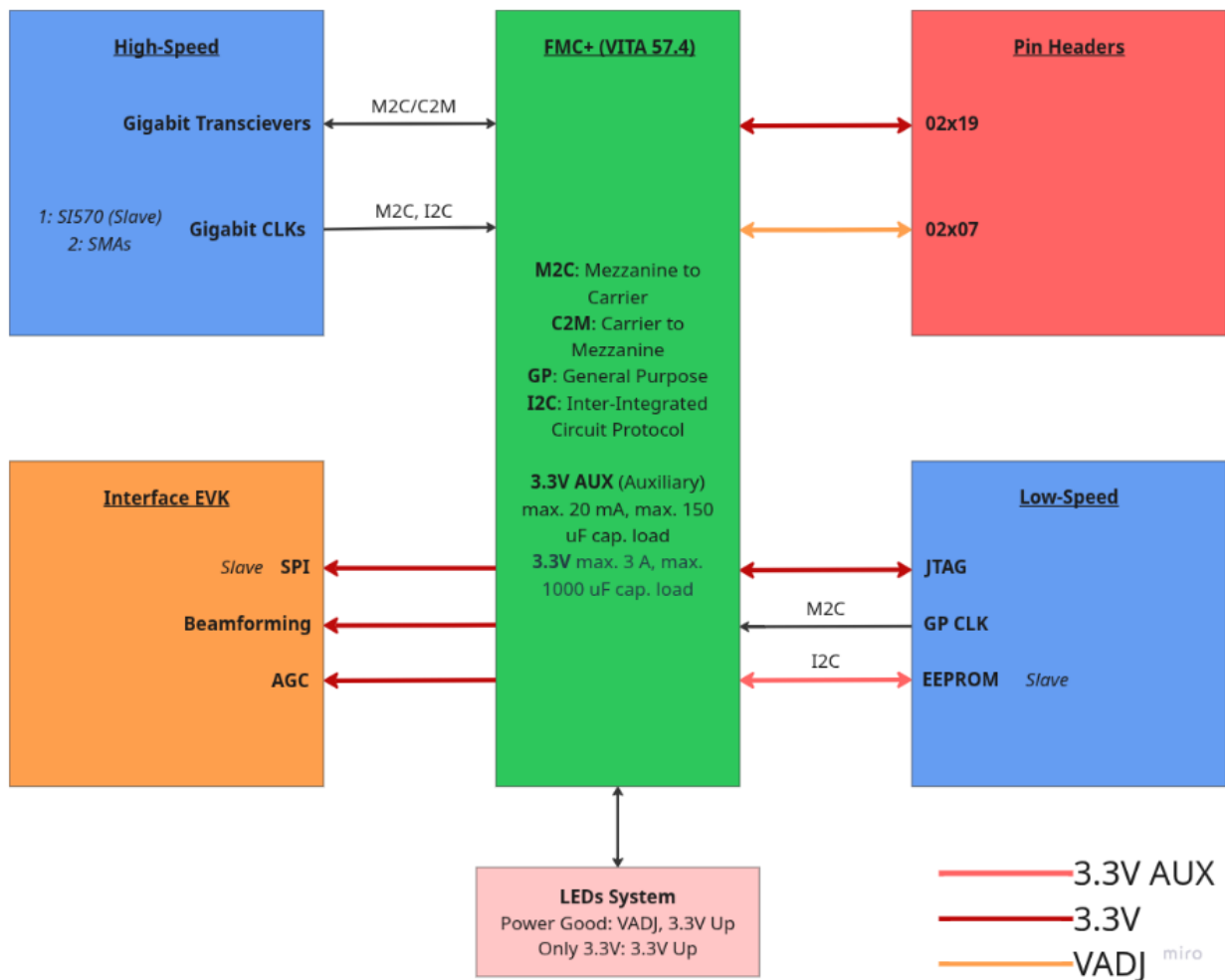


Figure 1: High-level Block Diagram of SENS of Doom.

## 2.3 System Requirements

We outline the key requirements for SENS of Doom.

ID	Title	Description
LR_BB_001	Mechanical	The PCB must not exceed a width of 7.8 mm to fit into the ZCU208 Evaluation Board.
LR_BB_002	VADJ Power Rail	The ZCU208 must be able to read an I2C EEPROM on the Mezzanine to configure the VADJ voltage rail, following VITA 57.4 Standard.
LR_BB_003	EEPROM Specifications	The PCB must feature an I2C EEPROM powered by the auxiliary 3.3V, and must consumes less than 7mA.
LR_BB_004	Sivers Interfaces	SENS of Doom must connect to the external SPI, BF and AGC interfaces of the Sivers EVK06005.
LR_BB_005	Impedance Control	100 $\Omega$ differential impedance must be respected on all differential signals. In addition, SMA connectors must be rated at 50 $\Omega$ impedance.

Table 1: System Requirements for SENS of Doom.

### 2.3.1 Technical Specifications

	Unit	Value
Maximum Current on 3.3V rail	<i>A</i>	3, max. 1000 uF cap. load
Maximum Current on 3.3V AUX rail	<i>mA</i>	20, max. 150 uF cap. load
Dimensions	<i>mm * mm * mm</i>	XX*XX*XX

## 2.4 XDC Constraints

Xilinx Design Constraints (XDC) are a set of commands used in Vivado to define physical and timing requirements for FPGA designs. Any FPGA pin that needs to be routed in or out has to explain what logic to apply and which bus to use for example. The capabilities of each pin are provided by AMD/Xilinx in the *master constraint* file denoted by **XTP653**. We provide in Table [10] the pin mapping for XDC constraints.

## 2.5 Electrical Components

### 2.5.1 FMC+ Female Connector

The ZCU208 exposes its FPGA-side through the FMC+ HPC connector J1, which is a 560-pin Samtec connector with no breakout to any standard pin header, as described in the introduction. A complete summary of pin's purposes is shown on Table [10], following the description of [2]. It's important to understand that not all pins of FMC+ are driven by the XCZU48DR.

### 2.5.2 EEPROM and VADJ

Four pins of the FMC+ are dedicated to supply external devices through a configurable power rail: VADJ. The standard gives the opportunity to the Carrier to program this voltage level between 1.2V, 1.5V and 1.8V. The ZCU208 uses a Texas Instrument MCU MSP430 (called the System Controller) to control this, among other things. There are two important considerations:

1. At power on, the System Controller detects if a FMC+ module is plugged. If yes, it reads it's EEPROM by I2C to find a VADJ voltage level supported by the ZCU208 and the Mezzanine. If no EEPROM is found, the voltage level is set to 0V. On the ZCU208, this voltage level defines the power rail named VADJ\_FMC. The documentation of the ZCU208 explains that VADJ\_FMC, by default 1.8V, powers FPGA banks (64 and 67) which it's signals are driven towards the FMC+. 0V on this rail means that no signals can be used on this bank. Requirement LR\_BB\_002 is here to define a non-0V voltage level on this rail.
2. A System Controller user interface allows to set an explicit value for the VADJ\_FMC rail. Override mode is useful for Mezzanine cards that do not contain valid EEPROM data defined by the ANSI/VITA57.4 specification. This GUI works only on Windows, even if Linux is mentioned.

SENS of Doom features a small 2kB I2C EEPROM: M24C02-RMN6TP (U1), which is a non-volatile memory chip. This component has also the prefix of IPMI FRU, for Intelligent Platform Management Interface Field Replaceable Unit. The I2C interface is connected through the FMC+, and acts as a Slave. To communicate with it, the XCZU48DR exposes a built-in I2C Master interface. The EEPROM is powered via the 3.3V AUX.

The GA0 and GA1 pins (Geographical Address) are two address-selector signals driven by the carrier and used to assign each FMC+ slot a unique I<sup>2</sup>C address for its FRU EEPROM. The carrier hardwires these pins to a fixed 2-bit value per slot (e.g., 00, 01, 10, or 11), and the mezzanine routes them to the address-select inputs (A0, A1) of its EEPROM. The chip's effective I<sup>2</sup>C address becomes  $0x50 | (GA1 \ll 1) | GA0$ , allowing multiple mezzanines on the same I<sup>2</sup>C bus to coexist without conflicts. On the ZCU208, both GA0 and GA1 are tied to ground, so the EEPROM responds at the base address 0x50.

Even if Bank 68 is driven at 1.2V, the line can be driven towards the 3.3V-driven I2C EEPROM because of a PCA9306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator on the lines.

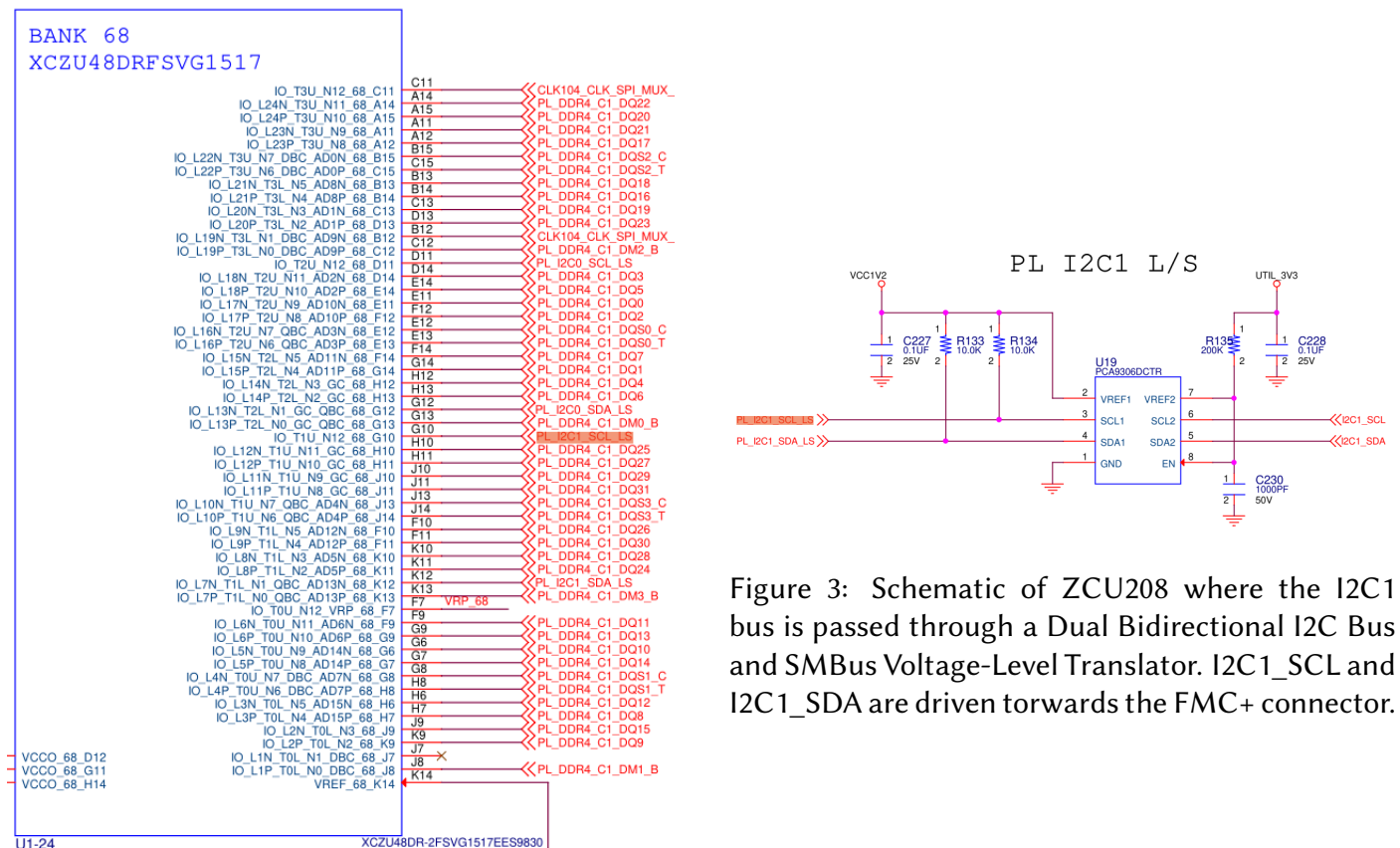


Figure 2: Schematic of Bank 68 (driven at 1.2V) of XCZU48DR, with I2C1 bus highlighted.

Figure 3: Schematic of ZCU208 where the I2C1 bus is passed through a Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator. I2C1\_SCL and I2C1\_SDA are driven towards the FMC+ connector.

### 2.5.3 GTY High-Speed Transceivers and SI570

GTY are high performance transceivers for optical and backplane applications, and provides data rates up to 30.5Gb/s [1]. The XCZU48DR exposes the Bank 130 towards the FMC+, which drives these signals. Out of the 4 M2C and C2M differential pairs available, SENS of Doom interfaces the DP0 and DP4 (C2M and M2C), using 8 Amphenole 132134 SMA through hole connectors, at 50  $\Omega$ .

In addition, 2 Multi-Gigabit differential clocks are exposed on Bank 130, but only for M2C. SENS of Doom gives the opportunity for the developer to

- Program a low-jitter I2C XO differential clock, between 10 and 810 MHz, through the SI570BCB, at 3.3V LVDS.
- Input his low-jitter differential clock through Amphenole 132134 SMA connectors (J6/J7) and right cables.

Similarly to the I2C interface of the EEPROM, the SI570 can be access by using the built-in I2C Master Interface of the Zynq. The SMA connectors are all capacitor serie coupled as high pass filter, 100 nF.

### 2.5.4 Phased Array Interfaces (SPI, BF, AGC)

SENS of Doom is primarily designed for interfacing with the EVK06005 phased array through its SPI, Beamforming (BF) and Automatic Gain Control (AGC) interfaces (Tables [2], [3], [4]). To facilitate the connectivity, the user manual of the phased array recommends to use 8-pin Molex 51021-0800 connectors, and use the Molex 0151340801 cable to connect both ends.

The pinout of these connectors are fully defined by the user manual of the phased array. The signal level should be 3.3V on each connector because these levels will be shifted down to 1.8V on the phased array.

Pin	Signal
8	GND
7	EVK_PWN_EN
6	EVK_EN_N
5	EVK_SPI_CLK
4	EVK_SPI_MOSI
3	EVK_SPI_MISO
2	EVK_SPI_CS_N
1	3.3V

Table 2: SPI pinout (J5).

Pin	Signal
8	GND
7	EVK_TX_RX_SW
6	EVK_BF_RST
5	EVK_BF_INC
4	EVK_BF_RTN
3	X
2	X
1	3.3V

Table 3: BF pinout (J4).

Pin	Signal
8	GND
7	EVK_AGC_RST
6	EVK_AGC_START
5	EVK_AGC_G0
4	EVK_AGC_G1
3	EVK_AGC_G2
2	EVK_AGC_G3
1	3.3V

Table 4: AGC pinout (J15).

### 2.5.5 Pin Headers

In addition to the EVK interfaces, SENS of Doom provides two interfaces for general purpose LA pairs. 12 pairs are available through J16 and J21, including one clock-capable. J16 and J21 both incorporate ground pins for signal integrity, and power pins at VADJ and 3.3V respectively. Tables [5] and [6] summarizes this.

### 2.5.6 JTAG Debug

The FMC+ allows any Mezzanine to debug Carriers through a JTAG interface (J2), highlighted by Table [7].

Pin	Signal	Signal	Pin
1	GND	GND	2
3	GND	GND	4
5	LA26_N	LA18_CC_P	6
7	LA26_P	LA18_CC_N	8
9	GND	GND	10
11	GND	GND	12
13	VADJ	VADJ	14

Table 5: J16 pinout.

Pin	Signal	Signal	Pin
1	GND	GND	2
3	GND	GND	4
5	LA29_N	LA28_P	6
7	LA29_P	LA28_N	8
9	GND	GND	10
11	LA24_N	LA31_P	12
13	LA24_P	LA31_N	14
15	GND	GND	16
17	LA25_N	LA30_P	18
19	LA25_P	LA30_N	20
21	GND	GND	22
23	LA21_N	LA33_P	24
25	LA21_P	LA33_N	26
27	GND	GND	28
29	LA22_N	LA32_P	30
31	LA22_P	LA32_N	32
33	GND	GND	34
35	GND	GND	36
37	3.3V	3.3V	38

Table 6: J21 pinout.

Pin	Signal	Signal	Pin
1	TCK	GND	2
3	TDO	X	4
5	TMS	3.3V	6
7	3.3V	X	8
9	TDI	GND	10

Table 7: JTAG pinout (J2).

### 2.5.7 LEDs System

The current-limiting resistor for a LED is sized using Ohm's law applied to the voltage dropped across the resistor

$$R = \frac{V_s - V_f}{I_f}, \quad (1)$$

where  $R$  [ $\Omega$ ] is the resistance,  $V_s$  [V] the supply voltage,  $V_f$  [V] the forward voltage, and  $I_f$  [A] is the forward current of the LED. For green LEDs, we want typically  $V_f \approx 2V$ , and go with a 20 mA as forward current. SENS of Doom features 3 green LEDs, each with  $V_f = 2.2V$ . For the 3.3V power rail and the PG\_C2M signal,

$$R = \frac{3.3V - 2.2V}{0.002A} = 550\Omega \rightarrow 560\Omega.$$

The PG\_C2M enables us to know if all power rails on the Mezzanine are functional. We additionally uses a third green LED for the 3.3V Auxiliary but with  $I_f = 5mA$ . This rail has a max. current of 20mA. We do not want to burn a big chunk of that budget on a LED when the whole point of it is to power the EEPROM:

$$R = \frac{3.3V - 2.2V}{0.0005A} = 2200\Omega \rightarrow 2k\Omega.$$

### 2.5.8 Power

To ensure noise suppression and power supply stability, power pins are equipped with a 100 nF capacitor, supplemented by a 10  $\mu$ F capacitor positioned as closely as possible to the chips for optimal effect.

## 2.6 Layout

This section outlines the PCB layout design, explaining the strategic decisions involved in the arrangement of components, the routing of traces, and the selection of layer stack-ups.

### 2.6.1 Controlled Impedance

SENS of Doom is a 6-layer PCB composed of 3 signal layers and 3 ground layers to minimize the returned path from high-speed signals. To properly keep a  $100\ \Omega$  differential impedance over all differential pairs across the PCB, track sizes and spacings have been carefully computed using a well-known calculator from JLCPCB. By using the recommended PCB thickness for a 6-layer PCB (1.6mm), and selecting the correct signal layers where differential pairs will be routed (L1, L3 and L6), we used

1. L1, L6: 0.12mm width, 0.2mm spacing
2. L3: 0.11m width, 0.2mm spacing

L1 and L6 have the same values because of their ground references that are symmetric in the stack-up. The full stack-up is shown on Table [8]. The PCB manufacturer can refer to the stack-up using its reference number JLC06161H-3313.

Layer name	Component	Thickness
Solder mask (top)	–	0.020 mm
Layer 1 (signal, power)	Copper	0.0350 mm
Dielectric 1	PrePreg FR4-7628	0.0994 mm
Layer 2 (ground)	Copper	0.0152 mm
Dielectric 2	Core FR4	0.5500 mm
Layer 3 (signal)	Copper	0.0152 mm
Dielectric 3	PrePreg FR4-7628	0.1088 mm
Layer 4 (ground)	Copper	0.0152 mm
Dielectric 4	Core FR4	0.5500 mm
Layer 5 (ground)	Copper	0.0152 mm
Dielectric 5	PrePreg FR4-7628	0.180 mm
Layer 6 (signal)	Copper	0.0994 mm
Solder mask (bottom)	–	0.0350 mm
<b>Total thickness</b>		<b>1.660 mm</b>

Table 8: SENS of Doom stackup.

### 2.6.2 Routing Differential Pairs

When routing differential pairs, several constraints must be respected to preserve signal integrity. The two traces of a pair should be routed in parallel and kept as close to each other as possible to minimize noise, while maintaining a controlled impedance by carefully sizing the trace width and spacing relative to the reference plane. The pair should be routed over a continuous ground plane to ensure a clean return path, avoiding splits or discontinuities that would degrade the signal. Length matching between the two traces of a pair (intra-pair skew) is critical to prevent timing skew and conversion of differential signals into common-mode noise; for this purpose, KiCad's tuning tools were used to add meander patterns and equalize the

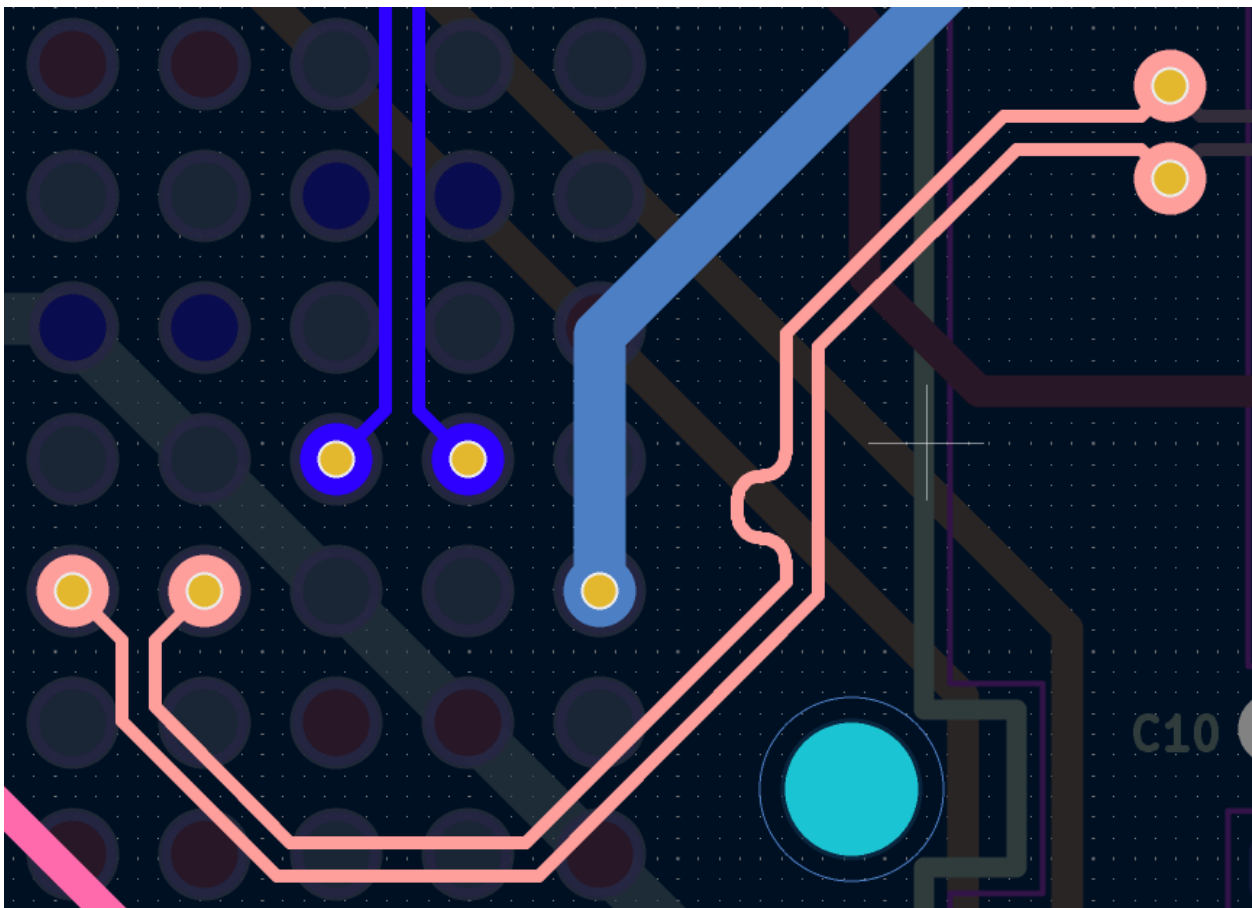


Figure 4: Example of tuning differential traces. The pale traces that come from the SI750 (Y1) have a matched length over L6. Sharp angles are avoided and the traces are routed symmetrically into and out of the pins/pads.

lengths within tight tolerances. When multiple pairs belong to the same bus (e.g., USB, Ethernet, or DDR lanes), inter-pair length matching was also applied to keep all signals synchronized. Additionally, sharp  $90^\circ$  angles were avoided in favor of  $45^\circ$  turns or arcs to limit impedance discontinuities and reflections, and vias along the differential path were minimized to reduce parasitic effects.

### 2.6.3 Physical Layout

The physical positions of components have been selected to respect both LR\_BB\_001 and LR\_BB\_005. SMA connectors for high-speed transceivers are isolated on the board to simplify routing, as shown on Figure [5]. The pin-headers, also differential, have pin's positions selected such that routing becomes simpler, shown on Figure [6].

## 2.7 Firmware

By being connected to the ZCU208, SENS of Doom is capable of using any built-in protocol interfaces provided, such as I2C and SPI. In particular, SENS of Doom wants to use the I2C1 bus to program its EEPROM. As explained before, the EEPROM responds to  $0x50$  but it has to take into account the TCA9548A Low-Voltage 8-Channel I2C Switch with Reset in the network. This switch enables identical I2C-addresses. The built-in driver XSpiPs of Xilinx has to enable the right path before sending any data. The TCA9548A for I2C1 bus has address  $0x75$ , and the FMC+ I2C bus is on channel 0. Following the datasheet of TCA9548A, the channel 0 has to be activated initially.

## References

- [1] AMD/Xilinx. *AMD High Speed Serial Technologies*. May 2026. URL: <https://www.amd.com/en/products/adaptive-socs-and-fpgas/technologies/high-speed-serial.html>.
- [2] FMC Hub. *VITA 57 FPGA Mezzanine Card (FMC) SIGNALS AND PINOUT OF HIGH-PIN COUNT (HPC) AND LOW-PIN COUNT (LPC) CONNECTORS*. 2026. URL: [https://fmchub.github.io/appendix/VITA57\\_FMC\\_HPC\\_LPC\\_SIGNALS\\_AND\\_PINOUT.html](https://fmchub.github.io/appendix/VITA57_FMC_HPC_LPC_SIGNALS_AND_PINOUT.html).

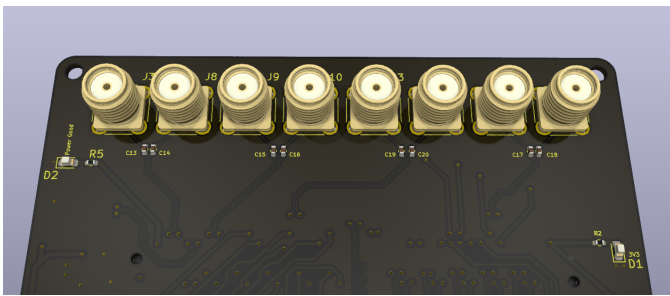


Figure 5: SMA connectors for high-speed transceivers are located on top of the board, isolated from everything.

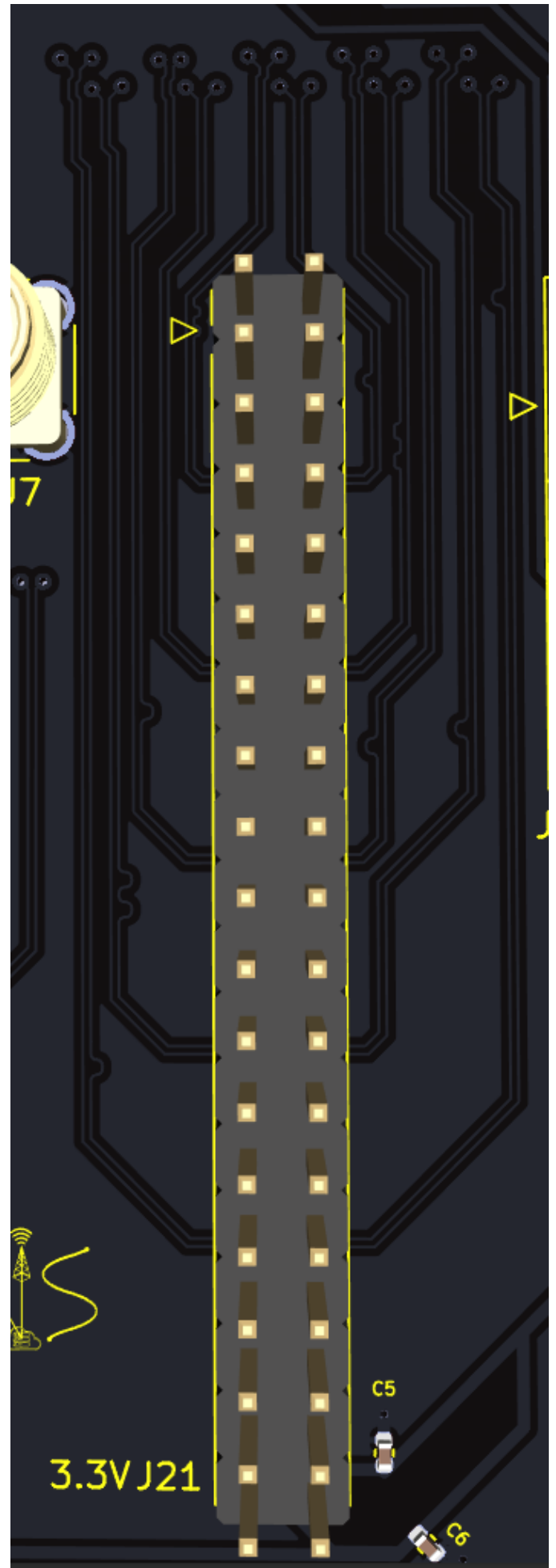


Figure 6: The 38-pin header is placed such that FMC+ pins for the LA bus are located closely to the connector, minimizing the path lengths.

Signal	Number of Pins	Clk-capable	Description
<i>High-speed data</i>			
DP_XX (M2C/C2M)	96	–	48 high-speed transceiver differential pairs (XX = 00–23 for C2M and M2C).
HA_XX (Bank A, HPC)	48	3 pairs	24 high-pin-count differential pairs on bank A.
HB_XX (Bank B, HPC)	44	3 pairs	22 high-pin-count differential pairs on bank B.
LA_XX (Bank A, LPC)	68	4 pairs	34 low-pin-count differential pairs on bank A.
<i>Clocks</i>			
GBTCLKX_M2C	12	yes	6 dedicated low-jitter multi-gigabit reference clocks for high-speed transceivers (X = 0–5).
CLKX_M2C and CLKY_BIDIR_M2C	8	yes	4 board-level differential clocks; two M2C (X = 0–1), two bidirectional (Y = 0–1) (direction set by CLK_DIR).
CLK_DIR	1	–	GND → M2C, 3.3 V via 10 k pull-up → C2M.
REFCLK_M2C / C2M	4	yes	Low-jitter reference clocks for data converters (ADC/DAC sample clocks).
<i>Control &amp; management</i>			
SYNC_M2C / C2M	4	–	Synchronization signals (e.g. JESD204B).
PG_M2C, PG_C2M	2	–	Power-good signals between carrier and mezzanine.
HSPC_PRSNT_M2C_L, PRSNT_M2C_L	2	–	Indicate that a mezzanine is connected. HSPC indicates its a High-Pin-Count.
GA0, GA1	2	–	Geographical address (I <sup>2</sup> C / EEPROM); driven by the carrier.
JTAG	5	–	Boundary-scan / debug interface.
SCL, SDA	2	–	I <sup>2</sup> C bus.
RES0–RES3	4	–	Reserved.
<i>Power &amp; reference</i>			
+12 V	5	–	12V power rail.
+3.3 V	5	–	3.3V logic supply.
+3.3 V AUX	1	–	Always-on auxiliary supply.
VADJ	4	–	Adjustable I/O supply, set by carrier-side regulator.
VREF_A_M2C, VREF_B_M2C	2	–	I/O reference voltages for banks A and B.
VIO_B_M2C	2	–	I/O supply for bank B, generated on the mezzanine.
GND	239	–	Ground returns.
<b>Total</b>	<b>560</b>		

Table 9: FMC+ connector pinout summary (560 pins).

FMC+ pin	FPGA bank	FPGA pin (P/N)	Board callout (P/N)	Purpose
<i>Bank 131 – GTY transceivers (FMC+ A/B)</i>				
DP4_C2M	131 (GTY)	D31 / D32	J11/J12	High-speed
DP4_M2C	131 (GTY)	E38 / E39	J13/J14	High-speed
GBTCLK1_M2C	131 (GTY)	P31 / P32	J6/J7	Low-Jitter Transceiver reference clock
<i>Bank 130 – GTY transceivers (FMC+ C/D)</i>				
DP0_C2M	130 (GTY)	H31 / H32	J3/J8	High-speed
DP0_M2C	130 (GTY)	J38 / J39	J9/J10	High-speed
GBTCLK0_M2C	130 (GTY)	U33 / U34	Y1	Low-Jitter programmable Transceiver reference clock
<i>Bank 67 – HP I/O – VADJ_FMC</i>				
LA00_CC_P	67 (LVCMOS18)	F21	J5	EVK_SPI_CLK
LA02_P	67 (LVCMOS18)	A20	J4	EVK_BF_INC
LA03_P	67 (LVCMOS18)	C21	J5	EVK_PWN_EN
LA04_P	67 (LVCMOS18)	C20	J4	EVK_BF_RST
LA05_P	67 (LVCMOS18)	F24	J15	EVK_AGC_START
LA06_P	67 (LVCMOS18)	E21	J15	EVK_AGC_RST
LA07_P	67 (LVCMOS18)	C23	J4	EVK_TX_RX_SW
LA08_P	67 (LVCMOS18)	E22	J4	EVK_BF_RTN
LA09_P	67 (LVCMOS18)	D23	J15	EVK_AGC_G1
LA10_P	67 (LVCMOS18)	J23	J15	EVK_AGC_G0
LA11_P	67 (LVCMOS18)	L19	J5	EVK_SPI_MOSI
LA12_P	67 (LVCMOS18)	J21	J5	EVK_SPI_MISO
LA13_P	67 (LVCMOS18)	J20	J15	EVK_AGC_G2
LA14_P	67 (LVCMOS18)	B24	J15	EVK_AGC_G3
LA15_P	67 (LVCMOS18)	B22	J5	EVK_RST_N
LA16_P	67 (LVCMOS18)	L24	J5	EVK_SPI_CS_N
CLK0_M2C	67 (LVDS)	G23 / H23	J17/J18	General-purpose LA clock
<i>Bank 64 – HP I/O – VADJ_FMC</i>				
LA18_CC	64 (LVCMOS18)	AM17/AL17	J16	Clock-capable LA pair
LA21	64 (LVCMOS18)	AU14/AU15	J21	General-purpose LA pair
LA22	64 (LVCMOS18)	AV13/AU13	J21	General-purpose LA pair
LA24	64 (LVCMOS18)	AN16/AN17	J21	General-purpose LA pair
LA25	64 (LVCMOS18)	AR16/AP16	J21	General-purpose LA pair
LA26	64 (LVCMOS18)	AW16/AV16	J16	General-purpose LA pair
LA28	64 (LVCMOS18)	AN15/AM15	J21	General-purpose LA pair
LA29	64 (LVCMOS18)	AR13/AP13	J21	General-purpose LA pair
LA30	64 (LVCMOS18)	AH17/AG17	J21	General-purpose LA pair
LA31	64 (LVCMOS18)	AJ15/AJ16	J21	General-purpose LA pair
LA32	64 (LVCMOS18)	AF16/AF17	J21	General-purpose LA pair
LA33	64 (LVCMOS18)	AH15/AH16	J21	General-purpose LA pair
<i>Bank 503 – JTAG – which voltage?</i>				
TCK	503 (PS)	AA29	J2	JTAG Clock
TDI	503 (PS)	AD31	J2	JTAG Data In
TDO	503 (PS)	AD32	J2	JTAG Data Out
TMS	503 (PS)	AD30	J2	JTAG Mode Select

Table 10: FMC+ to ZCU208 FPGA bank mapping with board-side callouts.

## A Other Signal Specifications

In this appendix, please find some explanations for signals that have not been taken into account in the design of SENS of Doom.

### A.1 VREF\_A

VREF\_A are reference voltage that the mezzanine or the carrier send to the other, used by certain I/O signaling standards on bank A. Some digital I/O standards don't just compare an input against ground. They compare it against a threshold voltage halfway between high and low. The receiver uses VREF as that threshold.

### A.2 VIO\_B

VIO\_B is a voltage that the mezzanine is expected to provide to the carrier, and the carrier uses it to power the FPGA's I/O bank that drives the HB bus pins. FPGA I/O banks need a supply voltage that matches the logic levels of whatever they're talking to. If the mezzanine has chips that run at 1.8 V logic, the FPGA's I/O bank driving those pins must also run at 1.8 V. If the mezzanine runs at 2.5 V, the bank needs 2.5 V. Rather than forcing the carrier to guess, the FMC+ spec says: "Mezzanine, you know what voltage your chips need — generate that voltage on your board and ship it back to us over the VIO\_B\_M2C pin. We'll use it to power the matching I/O bank on the FPGA."

### A.3 VADJ

VADJ is generated by a voltage regulator on the ZCU208 carrier board, not by the FPGA. The regulator is programmable — it can output different voltages depending on how it's commanded. On the ZCU208, the System Controller (a TI MSP430) is what commands the regulator.

### A.4 PG\_C2M

PG\_C2M is up when 3.3v, 12 and vadj are ok. Note there's a companion signal going the other way: PG\_M2C (Power Good, Mezzanine-to-Carrier). That's where your mezzanine tells the carrier "my onboard rails are good." If your mezzanine has its own regulators (e.g., to generate a 1.2 V core for an onboard chip), you'd drive PG\_M2C high once those rails are stable.

### A.5 REFCLK

REFCLK\_M2C and REFCLK\_C2M are high-quality, low-jitter reference clock pairs intended for data converters (ADCs, DACs) on the mezzanine, or for the FPGA's transceivers. FMC already had CLK0\_M2C, CLK1\_M2C, GBTCLK0\_M2C, etc. So why add more? The answer is jitter performance and purpose. Regular CLK\_M2C pins are general-purpose differential clocks — good for logic, timing references, etc. GBTCLK\_M2C pins are dedicated to the FPGA's GTY/GTH transceiver reference clock inputs — optimized for multi-gigabit serial links. REFCLK\_M2C/C2M are specifically for data converter sample clocks — the clock that drives an ADC's sample-and-hold or a DAC's output stage. These demand the lowest possible jitter because converter performance (SNR, SFDR) is directly limited by sample clock phase noise.

### A.6 SYNC

SYNC\_M2C and SYNC\_C2M are synchronization signals used to align multiple converters and transceivers in a deterministic way. They're defined for exactly two use cases: Use case 1: JESD204B SYNC signal JESD204B (the high-speed serial interface between converters and FPGAs) uses a SYNC signal to tell the transmitter "I'm ready to receive, start the initial link alignment sequence." This is a low-speed, single-ended signal (but routed as differential on FMC+).

## B Errors on PCB

SENS of Doom was initially designed with a JTAG connector. The right component was not in JLCPCB storage, so we ordered it without any component on the footprint. We found out that the board ordered like this will disable the JTAG-over-USB debug connection from Vivado when plugging the breakout board. This is because internally to the ZCU208 there is an analog switch (see Figure [7]). Because we really do not need any JTAG external connection, we shorted TDI and TDO on SENS of Doom, shown on Figure [??].

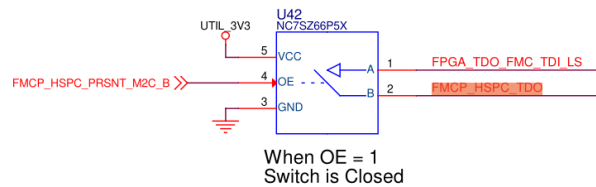


Figure 7: The signal *HSPC* comes from the Mezzanine. This analog filter disable in some way the JTAG-over-USB connection.

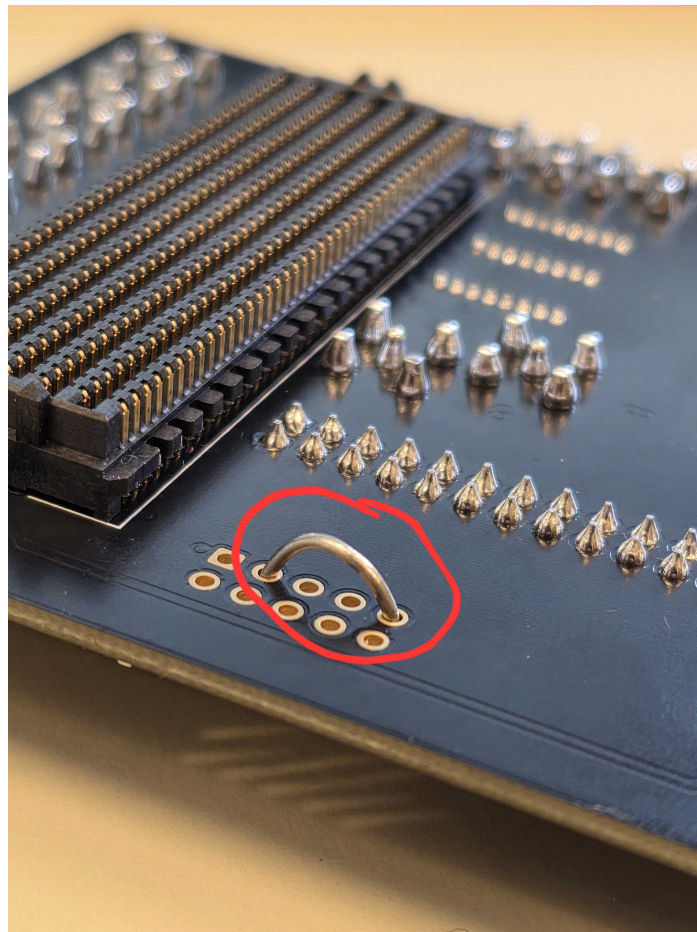


Figure 8: TDI and TDO of JTAG shorted.